CLAIMS

1. A process for forming a copper interconnect in a substrate including a connect hole vertically extending through an inter-level dielectric layer, comprising the steps of:

a first step, performed at least partially by atomic layer epitaxy, of depositing a barrier layer comprising tantalum on sides of said hole;

a second step, performed by physical vapor deposition, of depositing a copper seed layer over said barrier layer; and

filling by electrochemical plating copper into said hole over said copper seed layer.

2. The process of Claim 1, wherein said barrier layer comprises tantalum nitride.

3. The process of Claim 1, further comprising a third step performed between said first and second steps of etching said barrier layer at the bottom of said hole.

4. The process of Claim 3, wherein third step includes generating an argon plasma and biasing a pedestal electrode supporting said substrate to attract argon ions to said substrate, thereby etching said barrier layer.

5. The process of Claim 4, wherein said generating step includes inductively coupling RF power into a plasma reactor containing said pedestal electrode.

6. The process of Claim 1, wherein said first step includes an initial CVD step for depositing a first part of said barrier layer and a subsequent sputtering step for depositing a second part of said barrier layer.

7. A process for forming a copper interconnect in a substrate including a connect hole vertically extending through an inter-level dielectric layer, comprising the

sequentially performed steps of:

a first step, performed by chemical vapor deposition, of depositing a first barrier layer comprising tantalum on sides of said hole;

a second step, performed by sputtering, of depositing a second barrier layer comprising tantalum on said sides of said hole;

a third step, performed by physical vapor deposition, of depositing a copper seed layer over said first and second barrier layers; and

a fourth step, performed by electrochemical plating, of filling copper into said hole over said copper seed layer.

8. The process of Claim 7, wherein said chemical vapor deposition comprises atomic layer epitaxy.

9. The process of Claim 7, further comprising a fifth step performed after said first step performed in a sputter reactor of etching said first barrier layer at the bottom of said hole.

10. The process of Claim 9, wherein fifth step includes generating an argon plasma and biasing a pedestal electrode supporting said substrate to attract argon ions to said substrate, thereby etching said barrier layer.

11. The process of Claim 10, wherein said generating step includes inductively coupling RF power into a plasma reactor containing said pedestal electrode.

12. The process of Claim 7, wherein said chemical vapor deposition comprises atomic layer epitaxy.

13. A process for forming a copper interconnect in a substrate including a connect hole vertically extending through an inter-level dielectric layer, comprising the steps of:

depositing by a deposition process comprising chemical vapor deposition a

nitrided barrier layer on sides of said hole;

in a sputter reactor including a tantalum target, etching said nitrided barrier layer on a bottom of said hole;

in said sputter reactor, depositing a material comprising tantalum on sidewalls of said hole to form a second barrier layer;

depositing by physical vapor deposition a copper seed layer over said second barrier layer; and

filling by electrochemical plating copper into said hole over said copper seed layer.

14. The process of Claim 13, wherein said deposition process comprises atomic layer deposition.

15. The process of Claim 13, wherein said nitrided barrier layer comprises TiSiN.

16. The process of Claim 13, wherein said second barrier layer comprises TaN.